(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 544 127 A3**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **92118887.6**

(51) Int. Cl.5: **G06F 15/16**, G06F 15/80

(22) Date of filing: **04.11.92**

(30) Priority: **27.11.91 US 798788**

(43) Date of publication of application:
02.06.93 Bulletin 93/22

(84) Designated Contracting States:
AT BE CH DE ES FR GB IE IT LI NL SE

(88) Date of deferred publication of the search report:
20.04.94 Bulletin 94/16

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(54) **Dynamic multi-mode parallel processor array architecture computer system.**

(57) A Parallel RISC computer system is provided by a multi-mode dynamic multi-mode parallel processor array with one embodiment illustrating a tightly coupled VLSI embodiment with an architecture which can be extended to more widely placed processing elements through the interconnection network which couples multiple processors capable of MIMD mode processing to one another with broadcast of instructions to selected groups of units controlled by a controlling processor. The coupling of the processing elements logic enables dynamic mode assignment and dynamic mode switching, allowing processors operating in a SIMD mode to make maximum memory and cycle time usage. On and instruction by instruction level basis, modes can be switched from SIMD to MIMD, and even into SISD mode on the controlling processor for inherently sequential computation allowing a programmer or complier to build a program for the computer system which uses the optimal kind of parallelism (SISD, SIMD, MIMD). Furthermore, this execution, particularly in the SIMD mode, can be set up for running applications at the limit of memory cycle time. With the ALLNODE switch and alternatives paths a system can be dynamically achieved in a few cycles for many many processors. Each processing element and memory and has MIMD capability the processor's an instruction register, condition register and program counter provide common resources which are used in MIMD and SIMD. The program counter become a base register in SIMD mode. In one embodiment all instruction registers are coupled to form a common broadcast path, and in an alternative embodiment, the ALLNODE switch is utilized as an alternative path for broadcast to all processors coupled by the interconnection network to be chosen as the system of choice.

EP 0 544 127 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 92 11 8887

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	PROCEEDINGS OF THE 5TH INTERNATIONAL PARALLEL PROCESSING SYMPOSIUM 30 April 1991 , ANAHEIM, CA, USA pages 301 - 308 T. BERG AND H. SIEGEL 'Instruction execution trade-offs for SIMD vs. MIMD vs. Mixed Mode Parallelism' * page 301, right column, line 37 - page 302, left column, line 46 *	1,3,5, 12,28,37	G06F15/16 G06F15/80
D,A	US-A-4 873 626 (D. GIFFORD) 10 October 1989 * the whole document *	1-40	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 February 1994	Michel, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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EPO FORM 1503 03.82 (P04C01)